

DDR3 DIMM 2400 Interposer

For use with Keysight Logic Analyzers

FuturePlus Systems

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Power Tools for Bus Analysis

- Improved DDR3 2400MT/s bus analysis with shortest Interposer design available
- System cost reduction. Direct connection to Keysight U4154A logic analyzers eliminates need for 4 U4201A adapter cables.
- Includes automatic logic analyzer configuration software and protocol-decode software.
- Interposer design does not consume a slot
- Provides Clock Qualification using CKE0:1 and Reset



FS2361 DDR3 DIMM 2400 Interposer

Easy, Reliable DDR3 2400 Analysis

The FuturePlus® FS2361 DDR3 DIMM 2400 Interposer provides a mechanical, electrical and software interface between an Keysight logic analyzer and all signals on the DDR3 bus. The FS2361 is used to design and debug computer motherboards and DIMM's operating up to DDR3 2400 MT/s rates.

Key Features

- Quick and easy connection between the DDR3 DIMM SDRAM memory bus connector and Keysight logic analyzers
- Complete and accurate 2400 MT/s state and timing analysis up to 12.5 GHz
- Compatible with all 240-pin DDR3 SDRAM DIMM's up to 2400 MT/s.
- All signals are probed passively.
- Does not require U4201A cables, connections to the analyzer are built in
- RDIMM, UDIMM and LRDIMM are supported.
- Burst sizes of 4, or 8 are supported.
- Quick and easy setup using Keysight Eye Scan with 5 ps resolution

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Helping you Design Tomorrow's Computers, Today

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our Interposers and software help you monitor and verify complex activities on your advanced technology computer bus design. FuturePlus systems offerings include bus-analysis solutions for most popular computer buses. Visit www.futureplus.com for more information.

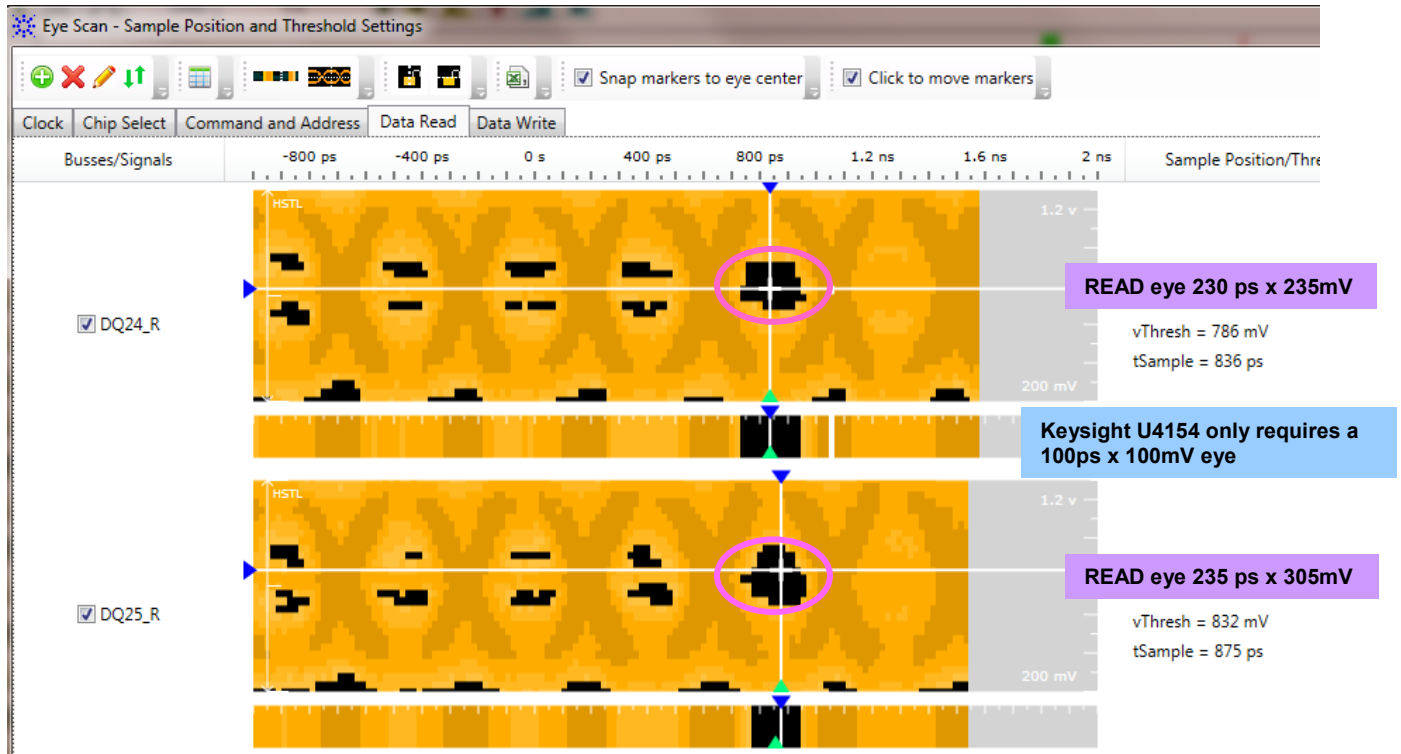


Strategic Solutions Partner

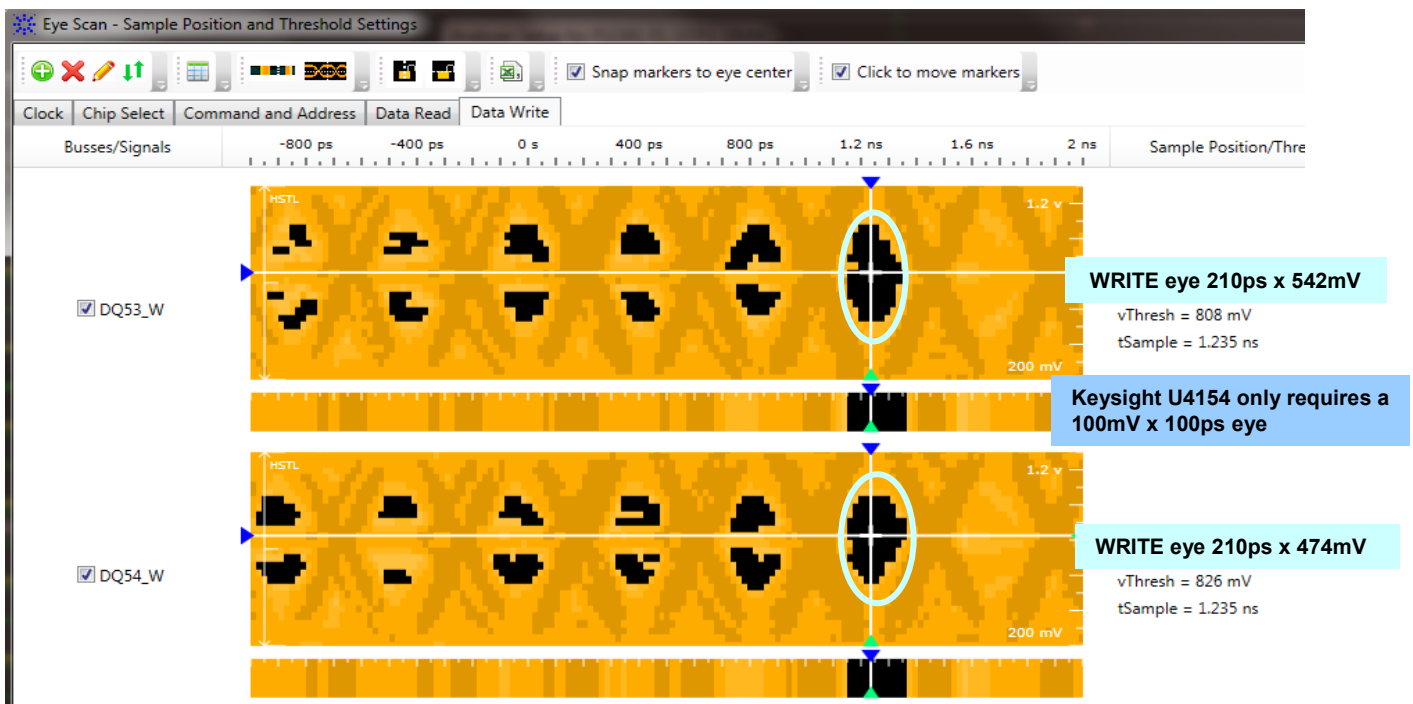
Since 1991

Demonstrated 2400 MT/s operation

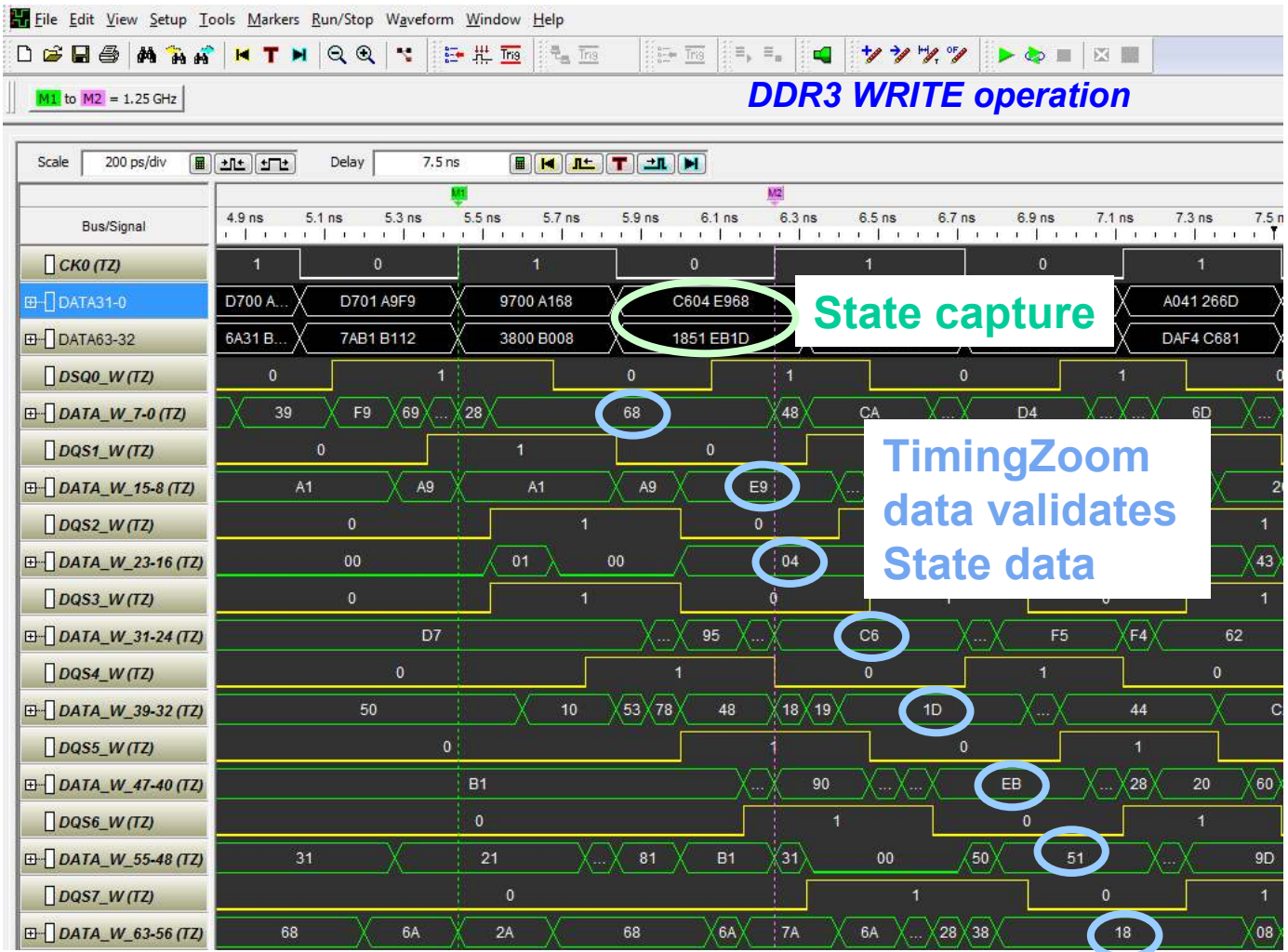
DDR3 2400 MT/s Data READ Eyes from Eye Scan display on the FS2361



DDR3 2400 MT/s Data WRITE Eyes from Eye Scan display on the FS2361



2400 MT/s State Capture



The FS2361 protocol-decode software translates acquired signals into easily understood bus transactions. This decode software executes in the logic analyzer to decode the DDR bus signals and present a display that lists the transaction type, address, data and command conditions.

User-selectable post-processing allows the acquired data to be displayed as different types of transactions in different colors.

Sample Num	Time	DDR3 Decoder:COMMAND	Cycle Type	ROWADDR	COLADDR
378	157.600 ns	DESELECT	NOT SELECTED	XXXX	XXX
379	158.080 ns		0000	12F0	2F0
380	158.480 ns	Read	READ	12F0	2F0
380.1		Bank = 2 Rank 0	0000		
380.2		Address = 288 02F0	0000		
380.3		Data = 2808B661 0300A878	0000		
380.4		Data = 280AB261 0300A878	0000		
380.5		Data = D13F5A45 CBDFBABF	0000		
380.6		Data = 93D8B19F D5AE3762	0000		
380.7		Data = B79BC74B 7E309AC6	0000		
380.8		Data = 59ED2BA1 E518E798	0000		
380.9		Data = 2F73EDE7 26FC154C	0000		
380.10		Data = 5E98C4EB 50A5622B	0000		
380.11			0000		
-3	-1.280 ns		0000		
-2	-800 ps	DESELECT	NOT SELECTED		
-1	-400 ps		0000		
0	0 s	Write	WRITE		
0.1		Bank = 6 Rank 0	0000		
0.2		Address = 280 02C8	0000		
0.3		Data = 1851EB1D C604E968	0000		
0.4		Data = C09D2044 F5B317CA	0000		
0.5		Data = 025773C2 628BFBD4	0000		
0.6		Data = DAF4C681 A041266D	0000		
0.7		Data = A313825D 50437055	0000		
0.8		Data = 2D3A52AD 3DFBF73	0000		
0.9		Data = 2C4CA6DE 0F26A92E	0000		
0.10		Data = FAF4FC77 A3E9A878	0000		
0.11			0000		

Quick and Accurate Setup

Get up and running quickly with Keysight EyeScan technology and the DDR Setup Assistant. A menu driven, step-by-step process guides you to setting bus timing parameters, voltage thresholds and individual sample positions easily.

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement of the design verification process. EyeScan lets you quickly acquire comprehensive signal integrity information on the DDR3 bus in your design, and can provide measurements with 5 ps of resolution.

Steps in DDR setup:

- Specify Input Parameters
- Verify Software Installation
- Load Configuration File
- Do Hardware Setup
- Set Initial Thresholds
- Set Sample Positions of Clk/CS Signals
- Set Sample Positions of Command/Addr Signals
- Find Latency Values
- Set Sample Positions of Data Read/Write
- Save Setup

Setting up: DDR3 -> DIMM Interposer

The first step is for you to provide some information about your target system, probing solution, and logic analyzer module.

Which logic analyzer module will you be using? FS2361 R1 DDR3 D1

What is the DDR bus type? DDR3

What probing solution are you using? DIMM Interposer

DIMM Interposer Model Number: --Select Model--

Overview

Probes: FS2361 R1 Interposer

Modules: Slots A-B [B], FS2361 R1 DDR3 DIMM

Tools: DDR3 Decoder

Windows: DDR3 Waveform, DDR3 Listing

[FS2361 R1 Interposer] General Purpose Probe Set

Probes used to connect to your Device Under Test

Reference Designator	Probe Type	Logic Analyzer Pod(s)
Lower[M] Pod 1	Custom 17-ch single-ended probe	Slot B Pod 1
Lower[M] Pod 2	Custom 17-ch single-ended probe	Slot B Pod 2
Lower[M] Pod 3	Custom 17-ch single-ended probe	Slot B Pod 3
Lower[M] Pod 5	Custom 17-ch single-ended probe	Slot B Pod 5
Lower[M] Pod 7	Custom 17-ch single-ended probe	Slot B Pod 7
Upper[S] Pod 1	Custom 17-ch single-ended probe	Slot A Pod 1
Upper[S] Pod 3	Custom 17-ch single-ended probe	Slot A Pod 3
Upper[S] Pod 5	Custom 17-ch single-ended probe	Slot A Pod 5

Dialog

Chip Select used: 1

Read Latency: 9

Write Latency: 7

Burst Length: 8

Data width to display: All 64 Bits

Number of Logic Machines: 1 Machine

Protocol: DDR3

CKE Qualification: No

Address Merging: No

Eye Scan - Sample Position and Threshold Settings

Busess/Signals: ADDR6, ADDR7

Time scale: -6 ns to 1 ns

Eye Scan - Sample Position and Threshold Settings

Busess/Signals: DQ24_R, DQ25_R

Time scale: -800 ps to 1.2 ns

Easy to set voltage thresholds and sample positions individually

Ordering Information (contact FuturePlus for a quote)

FS2361 – DDR3 2400 Interposer Probe of all A/C/C/DQ signals for use with Keysight U4154A Analyzers

FS236x – DDR3 2400 Interposer Probe of just A/C/C signals for use with Keysight U4154A Analyzers

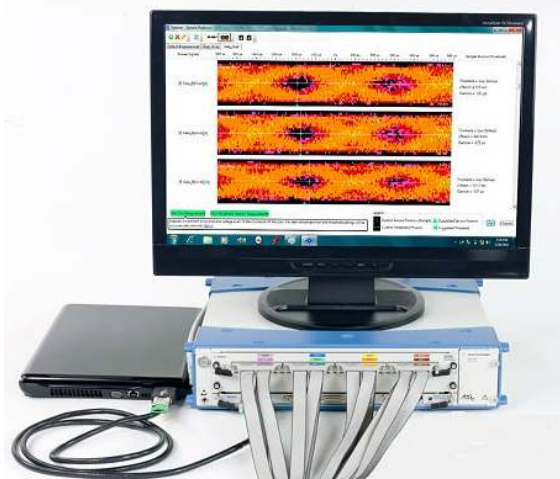
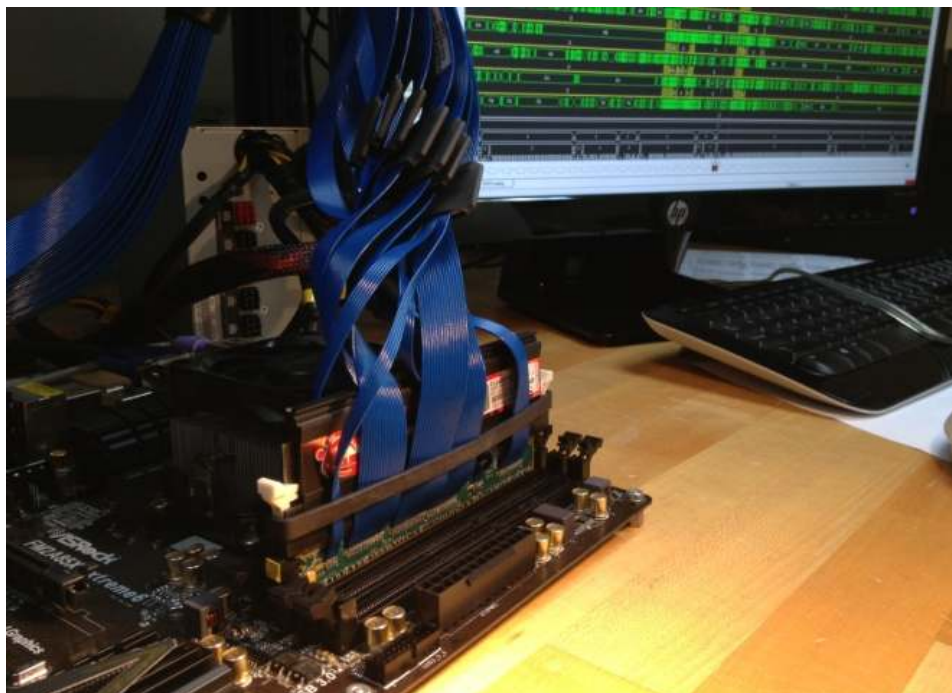
Software included :

Configuration files and licensed FS1136 Protocol Decoder software for the Keysight logic analyzer

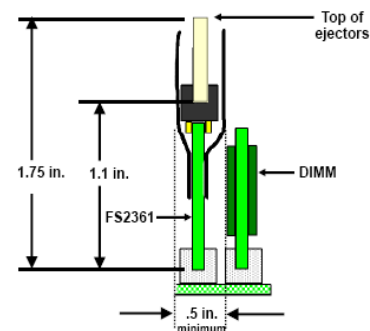
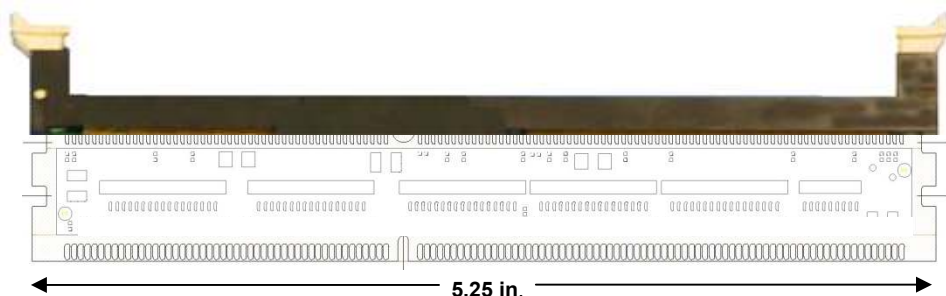
Keysight Logic Analyzer Requirements

The **FS2361** requires the **U4154A**. The requirements for 64 bit operation:

- Qty 1 M9502A two-slot AXIe chassis
- Qty 2 U4154A 136-channel Logic Analyzer Module (only 1 U4154A required for the FS236x)



FS2361 DDR3 DIMM interposer in a target system



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