**DisplayPort HBR3 Protocol Analyzer**

- The ONLY tool on the market that does not rely on a reference sink or source and monitors BOTH the high speed main link and the Aux channel!
- Complete packet by packet decode of the DisplayPort High Speed Main Link and Aux up to and including HBR3 8.1Gbit/s
- Includes protocol-decode software and probe configuration software
- Different target connection cables available, DP and USB Type C, flying lead and eDP probing
- Supports DP v1.1a, v1.2a, DP v1.3, DP 1.4 and eDP1.3
- Provides for optional upgrade for DSC/FEC, eDPv1.4b and Remote Software Interface
- Decodes and time correlates Aux and High Speed main link traffic
- Supports SST and MST traffic
- 16Gbyte Main Link trace buffer allows for multiple frame capture and pixel by pixel analysis
- Helps find the source of your CTS (Compliance Test Spec) failures!

**Key Features**

- Supports X1, X2, and X4 DisplayPort Versions 1.1a, 1.2, 1.3, 1.4 MST and SST Modes and eDP 1.3
- Data acquisition includes 8.1 GT/s
- Probe Manager software controls the FS4500 via a USB link and defines complex protocol aware filters
- Quad state LED’s display instant lane by lane activity status.
- Powerful Protocol Decode software decodes that displays Main Link and Auxiliary channel activity
- FS4507 Remote Interface allows for automated testing of your source and sink.
- No Requirement for a reference sink or reference source as the FS4500 works with ANY DP source and sink.

---

**Helping you Design Tomorrow’s Computers, Today**

FuturePlus Systems is the technology leader in protocol analysis tools for the computer design industry. Our products help you monitor and verify complex activities on your advanced-technology computer bus design. FuturePlus Systems offerings include bus-analysis solutions for most popular computer buses. Visit [www.futureplus.com](http://www.futureplus.com) for more information.

FuturePlus® is a registered trademark of FuturePlus Systems
DisplayPort High Speed Main Link Analysis

Easy and Quick Setup

Triggering on the exact DisplayPort event

Save only the events of interest in the 16Gbyte trace buffer

See details down to the exact pixel

www.FuturePlus.com
10b mode helps debug Phy level problems

Remove any events from the captured trace to help narrow down your problem!

www.FuturePlus.com
MSA packets are bounded by SS and SE symbols because they are considered secondary data packets. The Mvid and Nvid are 24 bit values used for stream clock recovery. Horizontal and vertical characteristics of the frame are found in the MSA packet. Pixel information such as Colorimetry format, number of bits per pixel and component format.

The MSA packet is inserted once per video frame during the video blanking period and is used by the DisplayPort receiver in reconstructing the stream.
Auxiliary Port Analysis

Trigger on command and/or address to find events quickly.

Aux Port traffic is presented in an easy to read format and time correlated to the High Speed Main Link so cause and effect can be quickly analyzed.
Aux Channel Decode

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Time</th>
<th>Decode</th>
<th>Aux_Trig_Stat</th>
<th>Byte_Count</th>
<th>HPD_Valid</th>
<th>HPD_Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>4914A</td>
<td>MAX DOWNSPREAD Max Downspread = Up to 5% Requires AUX channel handshake</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>61</td>
<td>4914A</td>
<td>Number of Receiver Ports = 1</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>62</td>
<td>4914A</td>
<td>Aux Read request, Address = 2 Length = 4</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>63</td>
<td>4914A</td>
<td>Aux ACK Max lane count = 4 lanes Enhanced Frame cap = 1 Training pattern sequence is not supported for 1.2</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>64</td>
<td>4914A</td>
<td>MAX DOWNSPREAD Max Downspread = Up to 5% Requires AUX channel handshake</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>65</td>
<td>4914A</td>
<td>Number of Receiver Ports = 1</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>66</td>
<td>4914A</td>
<td>Downstream Port Not Present Downstream Port type: DisplayPort Format Conversion (DCPD ver. 1.1)= No format conversion block Downstream port capability field = 1 byte per port, starting from address 000080h</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>67</td>
<td>4914A</td>
<td>Aux Read request, Address = 3 Length = 4</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>68</td>
<td>4914A</td>
<td>Aux ACK MAX DOWNSPREAD Max Downspread = Up to 5% Requires AUX channel handshake</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>69</td>
<td>4914A</td>
<td>Number of Receiver Ports = 1</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>70</td>
<td>4914A</td>
<td>Downstream Port Not Present Downstream Port type: DisplayPort Format Conversion (DCPD ver. 1.1)= No format conversion block Downstream port capability field = 1 byte per port, starting from address 000080h</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>71</td>
<td>4914A</td>
<td>MAIN LINK CHANNEL CODING DisplayPort Receiver does support Main link channel coding spec.</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>72</td>
<td>4914A</td>
<td>Aux Read request, Address = 4 Length = 4</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>73</td>
<td>4914A</td>
<td>Aux ACK Number of Receiver Ports = 1</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>74</td>
<td>4914A</td>
<td>Downstream Port Not Present Downstream Port type: DisplayPort Format Conversion (DCPD ver. 1.1)= No format conversion block Downstream port capability field = 1 byte per port, starting from address 000080h</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>75</td>
<td>4914A</td>
<td>MAIN LINK CHANNEL CODING DisplayPort Receiver does support Main link channel coding spec.</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>76</td>
<td>4914A</td>
<td>Downstream port count = 0 OUI supported</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

Aux Channel communicates configuration data between the monitor and the host PC.

Diagnostic mode information is also communicated over the Aux Channel.

Aux Channel is a bidirectional half duplex 1 Mb/sec communication channel.
Frame Display SW
Uses the pixels captured by the FS4500 to repaint the frame

Audio Packet Play SW
Audio Play Back Software takes the acquired Audio packets and plays them

Visit the FuturePlus Systems GitHub site for FREE source code!
https://github.com/FuturePlusSys/FS4500---VidAudFramer
Ordering Information

**FS4500** - DisplayPort v 1.1a/v1.2a/v1.4 and eDP1.3 Protocol Analyzer
**FS4504** - Add eDP 1.4b support FS4500
**FS4505** - DisplayPort v 1.1a/V1.2a/eDP 1.3 Protocol Analyzer
**FS4506** - Add DSC and FEC support to the FS4500
**FS4507** - FS4500 Remote Interface
**FS4510** - DisplayPort v 1.4 **Aux only** Protocol Analyzer

**HBR3,HBR2 and HBR 1.62, 5.4 and 8.1Gb/s probing**
**FS1046** - 1-4 Lane DP HBR3 Cable Repeater
**FS1045** - 1-4 Lane DP Snooper
**FS1047** - 1-4 Lane DP USB TypeC Snooper
**FS1049** - 1-4 Lane DP USB TypeC HBR3 Repeater

**eDP Probing**
**FS1090** - eDP 30 pin Repeater for the FS4500
**FS1091** - eDP 40 pin Repeater for the FS4500

Software included:
Probe Manager, runs on a Windows based laptop or PC, supports Windows 10 and earlier.

Note: The bit rate at which the probing will support is highly dependent on the target signal strength and quality.

---

**FuturePlus Systems Corporation**
15 Constitution Dr
Bedford, NH 03110-6042
Tel: 603 472-5905
Fax: 603 471-2738

Website: [www.futureplus.com](http://www.futureplus.com)
Email: Protocol.Decode@futureplus.com

FuturePlus Systems does not assume any responsibility for use of any circuitry described, and reserves the right to change circuitry and specifications at any time without notice. FuturePlus® is a registered trademark of FuturePlus Systems Corporation.